COGAR SYSTEM 4®

SYSTEM SUMMARY

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Designed

for users who require a total and daily commitment from their Data Processing Equipment.

The Cogar System 4® is a compact, operator oriented, general purpose data processing system. In a single desk-top unit, it combines magnetic tape transports, input keyboard, visual CRT display, I/O interfaces, solid state memory and a versatile processor.

The System 4 features transparency of coding and graphics, with all major functions under processor program control. Both the hardware and the software are designed to allow and assist operator interaction, while retaining sophisticated data manipulation capabilities.

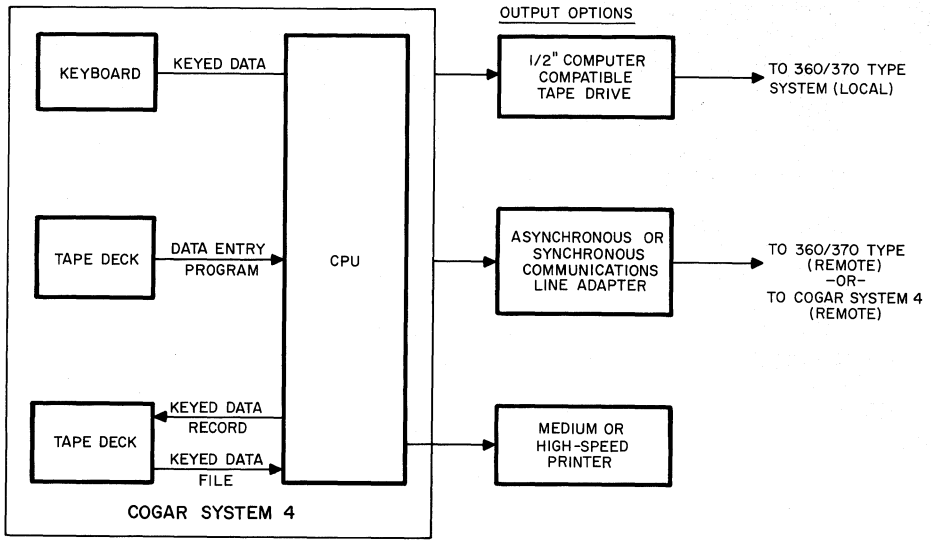
The processor architecture is designed to optimize byte handling and interpretation, and to provide automatic threading of recursive subroutines. Designed specifically for the efficient processing of graphics data, it incorporates a high performance byte-oriented processor, and a flexible, modularly expandable I/O system.

The application flexibility of the System 4 makes it a suitable building block in every type of installation, including data entry systems, communications terminals, small programmable processors, off-line printing stations, multifunction data stations, or as a full standalone EDP installation with complete peripheral complement.

The esthetic design of the System 4 is in complete accord with any office environment. It is simple for even the most unskilled operator to use. The use of the display to provide conversational interaction with the operator obviates the requirement for extensive training and allows the operator to be immediately at ease with the equipment.

System Applications

Applications range from conventional data entry to a full stand-alone data processing system capable of meeting the requirements of small and medium size installations. However, the System 4 is designed to grow right along with future application requirements. The easy-to-use instruction language allows the user to program it to perform new or specialized functions for unique applications. The system's design flexibility, technology, and simplicity ensure its staying power as a cost-effective tool.



DATA ENTRY APPLICATION

Data Entry

As a data entry device, the Cogar System 4 provides all the conventional features usually found in a data entry environment, plus the convenience and flexibility of operator interaction with the machine by providing a CRT display at every key station. A software system specifically designed for high-volume, validated data entry and verification is contained on a self-loading program tape. Three levels of program formatting are available, which may be interchangeably selected by the operator without reloading the program tape.

All keypunch functions, as well as all key-to-tape functions are standard. Functions like automatic skipping and duplicating, field balancing, automatic program selection, automatic formatting, sight or key verification, editing, blocking, and record searching.

Extremely reliable data storage, combined with powerful off-line data editing and validating capabilities result in virtual elimination of errors while the data is being keyed. A complete set of interlocks insure that the machine is prepared to accept the data before the operator can begin the keying-in process, thus eliminating procedural errors.

Programming Tool

The Cogar System 4 provides the program designer with a unique software tool which allows program design and debugging to be carried out interactively The standard programming language of the System 4 functions at several different interlocking levels and may be used in whatever mode best suits the programmer or the application. Programs may be created in Object language or in Symbolic language, using only the System 4 processor. The program may then be examined visually, individual instructions may be modified, or entire sections or subroutines within the program may be rearranged. The machine thus allows the programmer the option of fragmenting and restructuring his program without intervening action by peripheral assemblers or other equipments. This capability provides unprecedented flexibility and economy in the performance of program editing and debugging, as well as providing the ability to utilize existing subroutines in a program which is being newly-generated.

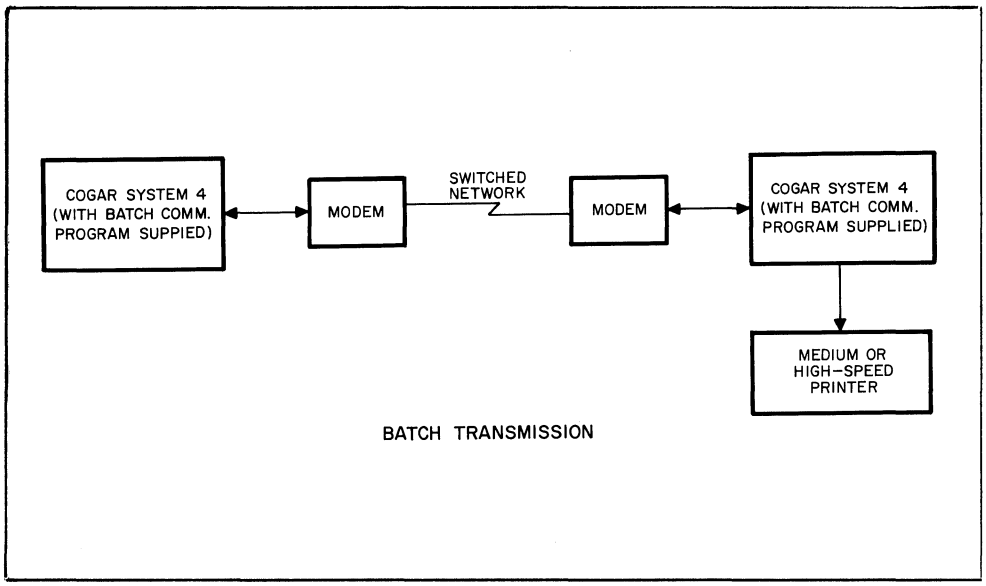
Remote Terminal

With its communications option, the Cogar System 4 becomes an intelligent remote terminal. The processor's ability to handle editing, formatting, communication, calculation, control and decoding duties can mean considerable savings in central computer and communication line time. Varieties of communication options include: Batch Transmission, Bisynchronous Communications, Teletype Simulation and System 4 to Systems 360/370.

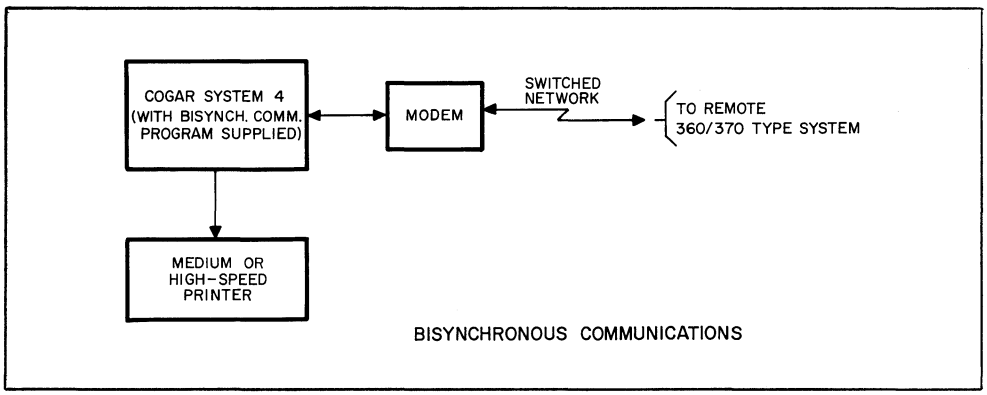
Using Batch Transmission, records and messages may be transferred from System 4 to System 4 over switched networks. The grade of the transmission line is continually sampled by the program and the transmission speed adjusted accordingly in the range of 1200 to 1800 baud. The package provides for full error detection, operator alert, and error recovery.

Using Bisynchronous Communications, the System 4 transfers data and messages over switched networks to a large computing system. Communication is in a high-speed, synchronous mode at transmission rates of 2000, 2400, and 4800 baud. Operator intervention during transmission, automatic answer, error detection and recovery are included.

In the Teletype Simulation mode, the System 4 can be dialed into any computer supporting remote teletypes (including another System 4), for exchange of data. Transmission over switched networks is at a speed of up to 60 characters per second.



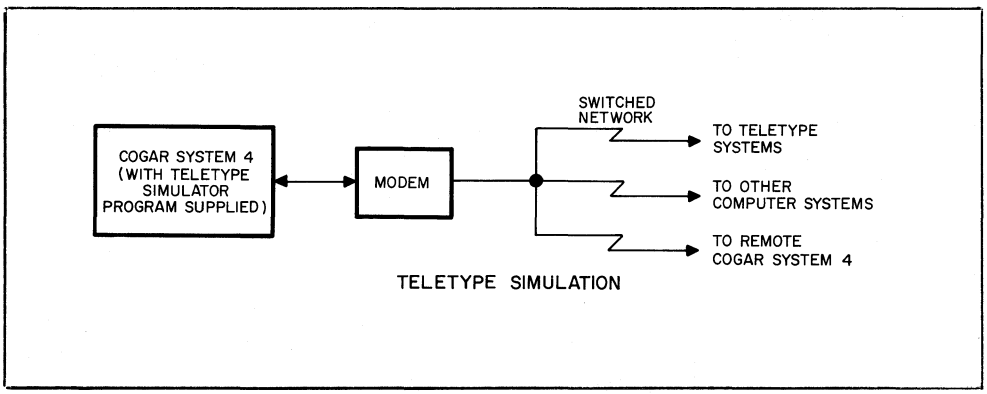
BATCH TRANSMISSION



BISYNCHRONOUS COMMUNICATIONS

System Controller

The System 4 offers an integrated operator interface as well as a versatile processor, so that implementation of larger special purpose systems using the System 4 as a controller can offer special advantages. Programmable component and logic testers are excellent examples of such applications.



TELETYPE SIMULATION

Education

The Cogar System 4, because it contains all the basic elements of a complete data processing system, makes an excellent teaching aid for computer concepts. It also can provide a good hands-on introduction to various programming languages.

Software

The Cogar System 4 is provided with fully supported software to make is immediately available for use in a variety of tasks. Pre-packaged programs provided by Cogar are stored on cartridge tapes and loaded into the machine as required by the user to perform specific functions. Master Function tapes are also provided, to allow the user to generate a custom-made program which may then be executed on the System 4 to perform tasks which are unique to the user's requirements. The Cogar software provides for interactive program design and debugging at several levels, including machine language.

The "Program Summary Catalog" which is available from the Cogar Software Distribution Center, gives a complete listing of the programs which are currently available, and a brief description of each. Detailed descriptions of the use of each program are also available from the Software Distribution Center.

Software Features

- Completely programmable
- Self-contained operating system
- Remote and local data communications
- Multiple language levels
- Byte-oriented processor
- Program interrupts
- Subroutine relocatability
- Extensive subroutine library

Software Packages

Basic Assembler Background Libraries Diagnostic Libraries

Data Entry Data Verify Tape Search 9 or 7 track computer compatible Editor

Program Trace Utility Cogar Batch Communications Bisynchronous Communication

Teletype Simulator Sort/Merge Package Dot Pattern Converter

High Speed Record Search General Ledger Print Gang Punch, and others.

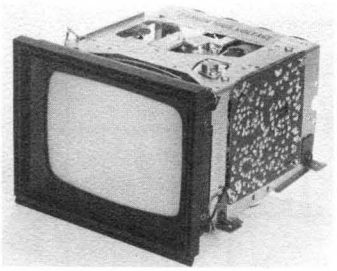
All software packages are operable on a 4K byte system.

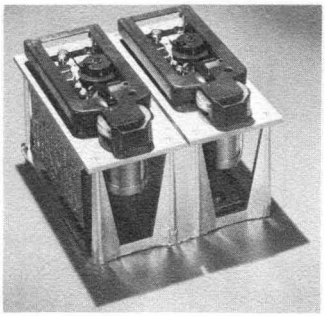
System Modularity

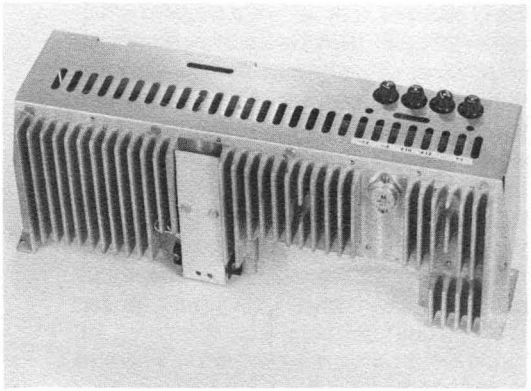
The superior reliability of the System 4 is the result of a modular packaging concept that eliminates internal wiring and complex interconnections that are the major cause of failures. Maintenance of any of the major components is simple. Four bolts are all that are required to remove and replace every major component. Each major sub-assembly is a functional entity permitting simple and rapid fault diagnosis and replacement.

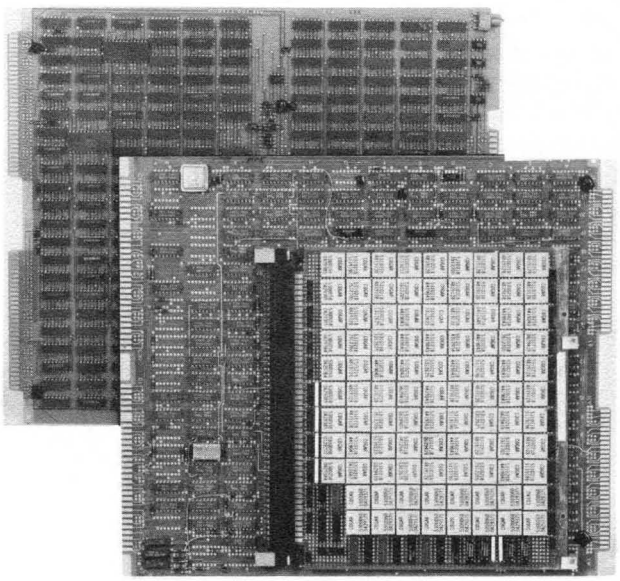
Cogar provides their customers a full capability in technical and systems support including training in field engineering and systems programming. Additionally, Cogar provides base level spare parts depots and repair services.

Product designs are implemented to provide for functional sub-assemblies which permit simple fault diagnosis and replacement. Functional sub-assemblies also permit more extensive in-process quality checks, enhancing the overall integrity and reliability of the total system. The packaging utilizes high-density, multi-layered printed circuit boards, minimizing the number of manually implemented interconnects. The casework and internal chassis are molded of lightweight, impact-resistant plastic, vacuum coated with metal to provide maximum safeguard against electrical interferences.







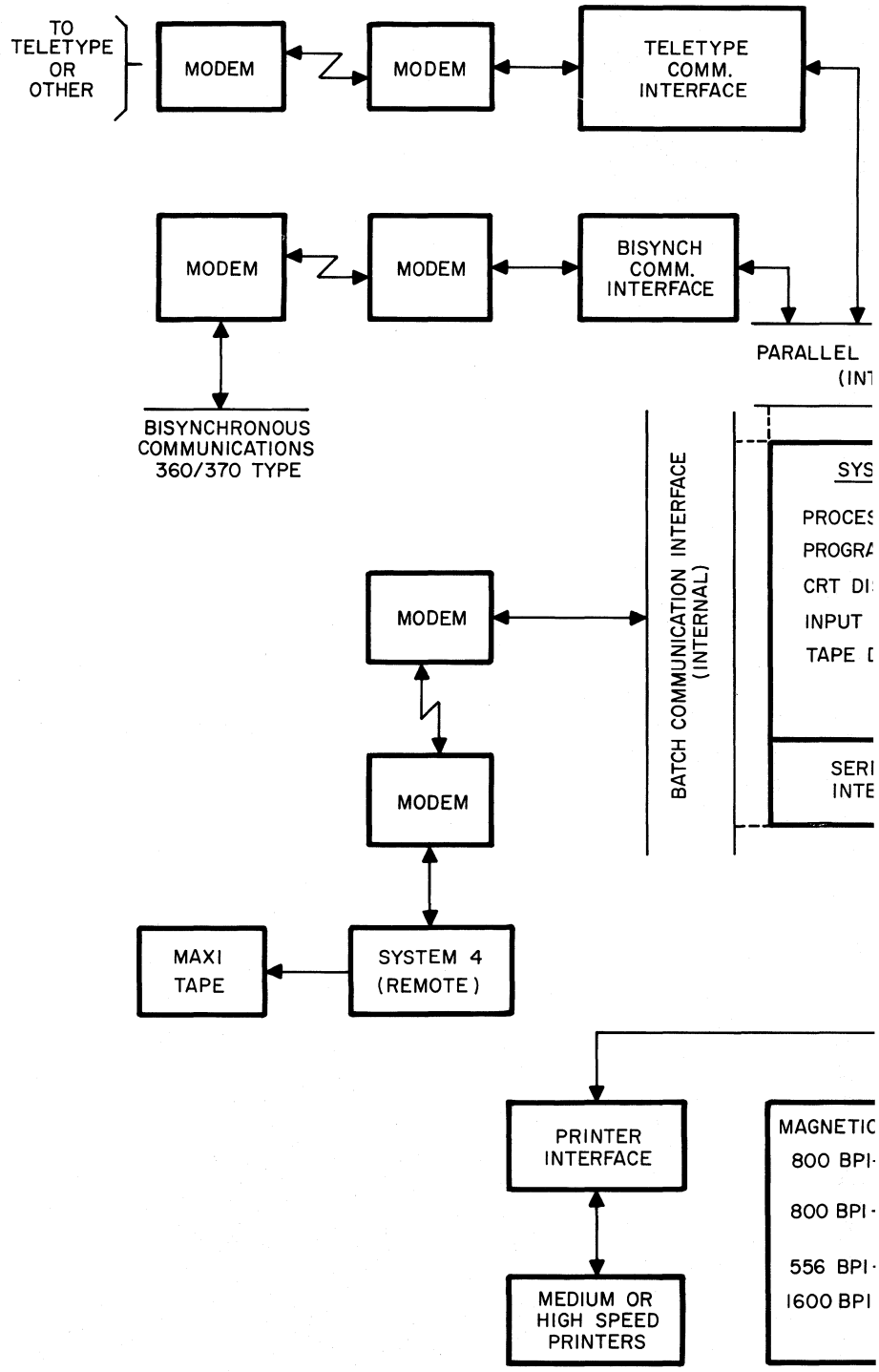


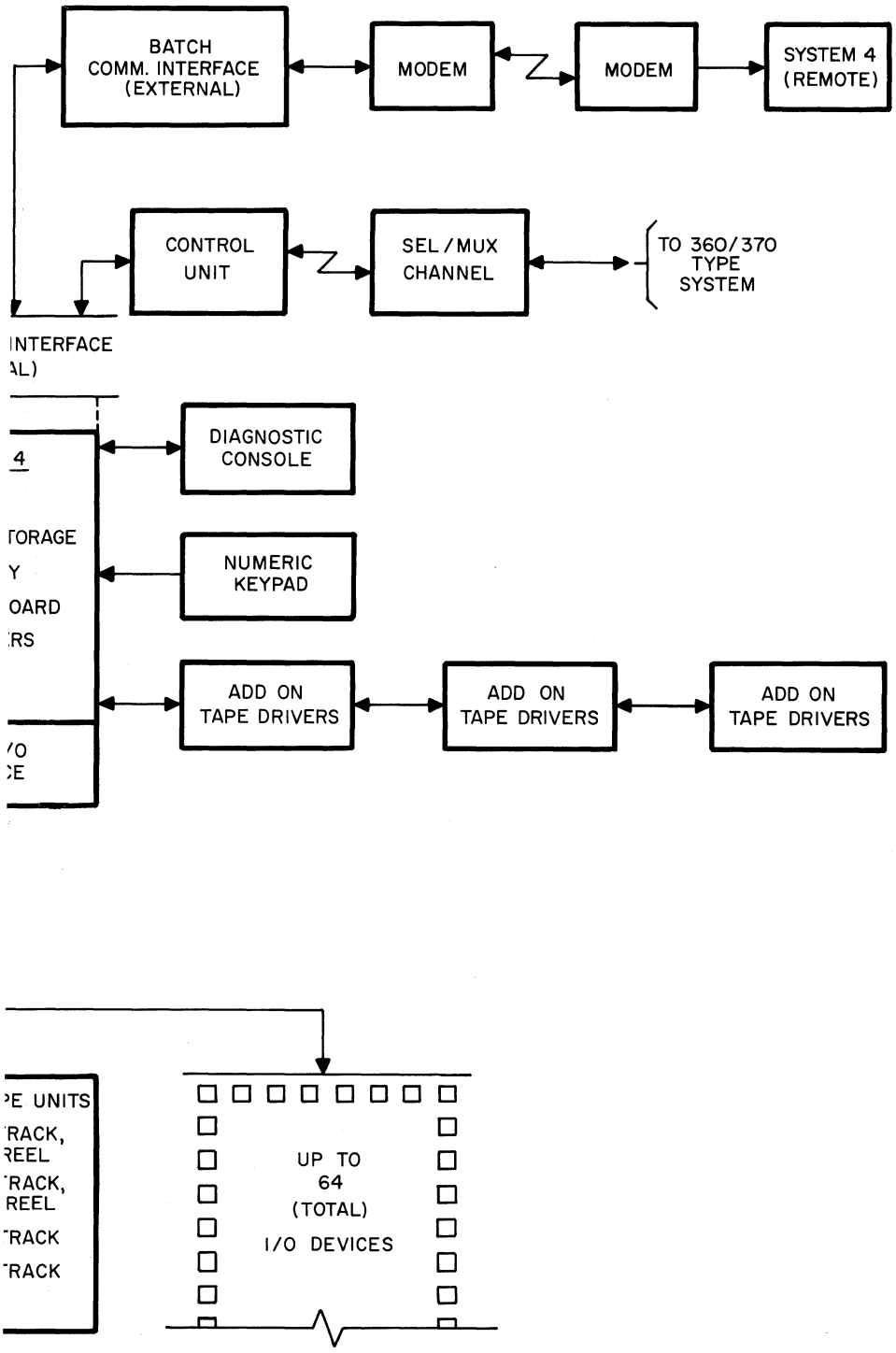
External Interfaces

The Cogar System 4 includes provision for three I/O interfaces. Included as a standard feature, a Serial I/O interface utilizing a single coaxial cable is connectable to up to 64 individual I/O devices. Data transfer on the cable is bidirectional, allowing one line to handle all activity. The use of high frequency, phase encoded techniques and address polling provides for system economy and flexibility without compromising reliability and thruput. The System 4 can transfer information to or from any one of the 64 peripheral devices at a rate of 58.8 kilobytes per second, in bit serial format. A wide variety of system configurations is easily realized. The use of a single coaxial cable permits reliable and economical attachment of peripheral devices through the Serial I/O Interface at distances of up to 1500 feet. In a system configuration where multiple System 4's are attached to the Serial I/O Interface through the coaxial cable, along with other I/O devices such as printers and computer-compatible tape drives, each System 4 may communicate with any other I/O device, under program control.

The Cogar peripherals designed to connect to the Serial I/O include:

- Magnetic Tape Units
  - 800 BPI, 9 Track, 7" Reel
  - 800 BPI, 9 Track, 10" Reel
  - 556 BPI, 7 Track
  - 1600 BPI, 9 Track
- Universal Printer Adapter
- Medium or High-Speed Printer
  - IBM 735
  - Centronics
- Additional System 4s





Additionally, the System 4 has the ability to accommodate up to four peripheral devices via a Parallel I/O channel, which can be operated by software *concurrent with the activities of the Serial I/O channel.* This optional communications interface connects to standard telephone datasets. The transmission rate is program selectable from 1200 to 2400 baud, and may be dynamically varied in response to communications line error rates. Communications to or from a local 360/370 system is accomplished through the multiplex channel link, or through the bisynchronous channel link for remote 360/370 communications.

The System also has an inherent provision for direct memory access, permitting transfer rates of up to one million bytes per second. This feature provides for multi-processor configurations with direct memory-to-memory interchange.

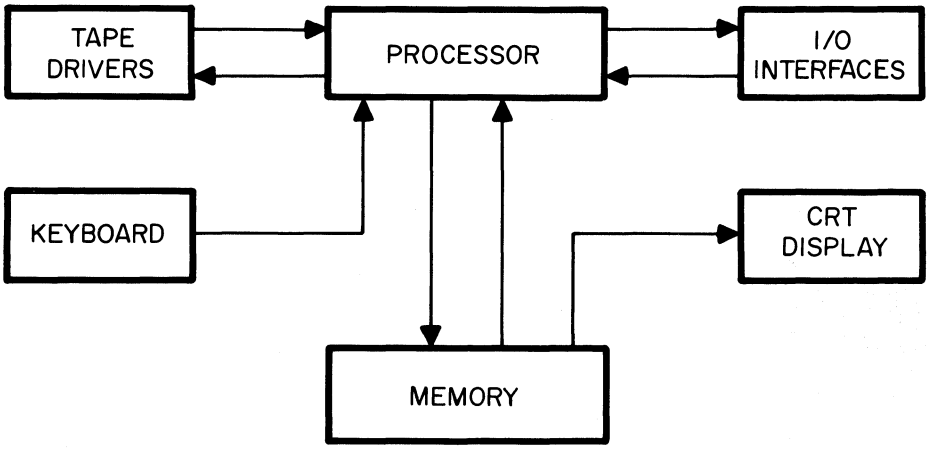
The flexibility of the system allows the user to add compatible peripherals and interfaces at will, without disrupting the processor configuration, and seldom any down-time in normal work activity.

System 4 to System 4 communications may be accomplished through the coaxial line of the Serial I/O channel, or through the Batch Transmission interface, for remote installation communications. The Batch Communications interface may be installed internally to the System 4, or may be installed in its external adapter enclosure.

System Organization

The Cogar System 4 is a self-contained data processing system. In its minimal configuration, it completely satisfies the requirements of a data capture system. As a media conversion device, any character which can be formed by a 5X8 matrix may be generated, without a change in the hardware. Performing as an intelligent terminal, it incorporates a high performance byte-oriented processor, along with flexibility in a modularly expandable I/O system.

The program controlled CRT display has direct access to memory. The keyboard, the tape drives, and the I/O interfaces gain access to memory through the processor. Interaction between the System 4 and the operator is accomplished through the display and the keyboard; therefore, no control panel is required. The two tape drives are used to enter and receive processor data and program material. The I/O interfaces provide bidirectional data paths for external peripheral devices, including special customer attachments. All major system functions are under the direct control of the processor program.



SYSTEM 4 – ORGANIZATION

System Options

In addition to the optional external peripheral devices which may be attached to the Cogar System 4, the following internal options may be specified. All of these options are factory installable only, and are configured within the standard System 4 package.

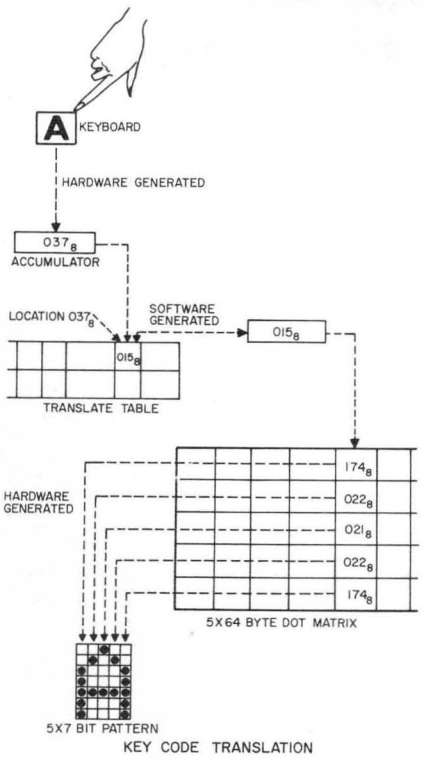
- Parallel I/O Interface
- Sense Switches
- 8K Byte Memory
- 16K Byte Memory

Keyboard

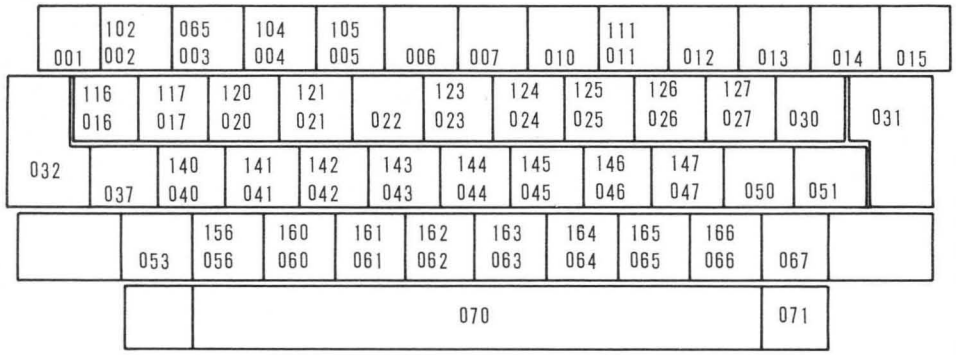
Many of the System 4 functions have been designed to be operated under processor control, in order to facilitate the customizing of the system to particular user applications. The codes generated from the keyboard for example, correspond to the physical *location* of the key, rather than to the character shown on the key. A translate table located in the processor memory is used to convert the key location code to the dot pattern for the character to be displayed. The translate table is completely programmable, and thus may be easily modified to produce any desired character configuration for any key location. This allows easy adaptation to particular keyboard configurations such as keypunch, typewriter, or teletype.

The system contains an inherent provision for N-key rollover, and the software provides for the formation of a keyboard queue, allowing keyboard input to be totally independent of other concurrent system operations. An acoustic transducer is included that may be set to sound a tone with every keystroke, or for silent keying, at the preference of the operator.

The illustration on this page shows the correlation of the key codes to the position of the keys. Actual data code assignment for each key is accomplished by table look-up techniques within the controlling software. For example, if the key for an "A" is depressed, an eight-bit octal code for Ø37 is generated. Location Ø37 (in the standard translate table) contains octal Ø15, which is the address of the character dot pattern for "A". This address is stored in an appropriate display buffer in memory, and is accessed each time that character is to be displayed.



KEYPUNCH KEYBOARD

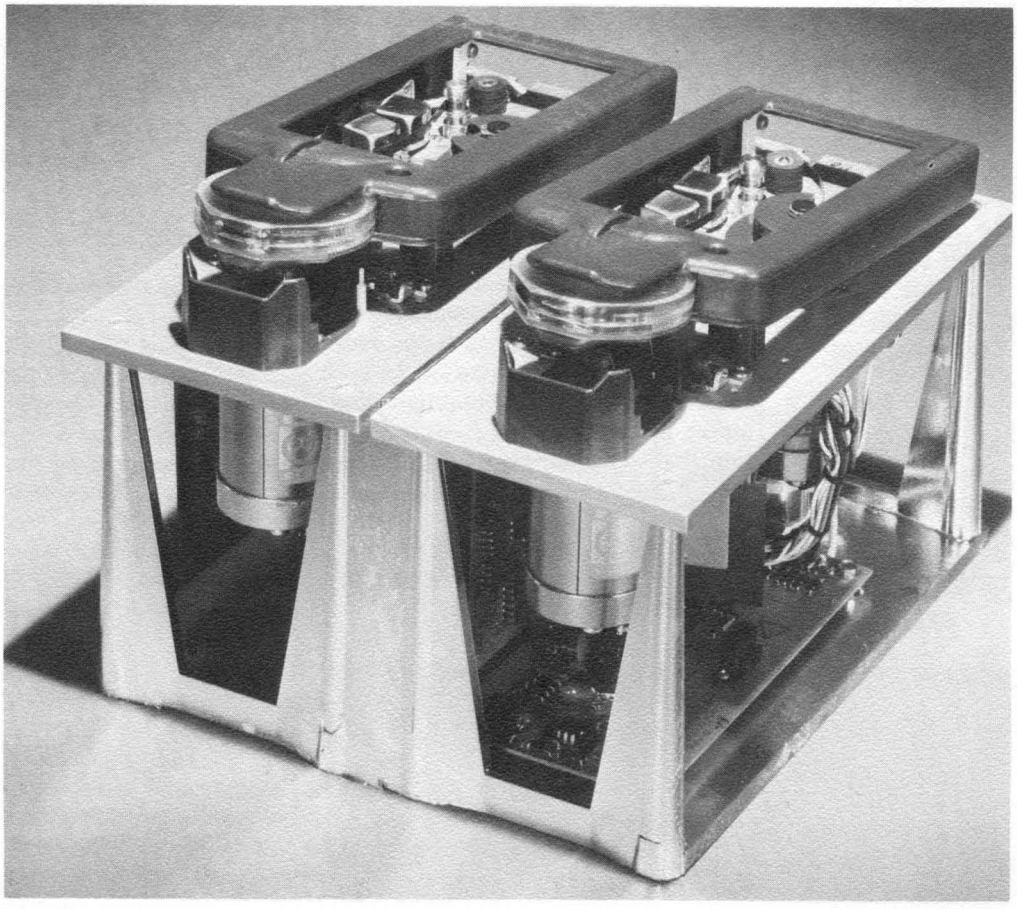


KEYBOARD KEY CODES

Visual Display

The visual display forms the primary channel of information from the processor to the operator. It consists of a 5 inch CRT, with its associated video electronics and addressing logic. Up to 256 characters may be displayed on the screen in 8 lines of 32 characters each. A 5 x 8 dot pattern may be displayed in each character position. The processor memory stores the dot pattern for each character type, and the screen is refreshed directly from the memory. With the display functions (including underline capability) under processor control, a programmer can directly manipulate not only the dot patterns available for display, but also which character code is associated with each pattern. The display has direct memory access with specifically assigned time slots to preclude impact on instruction execution times. Memory areas displayed are program selectable from any one of 16 memory pages (256 bytes per page), with provision for selective interlace of half pages. Provisions are included for cursor or underscore with selective blanking and an alternate graphic set which permits utilization of 128 unique graphics.

High Reliability
High Performance Tape Drives



- Servo controlled capstan drive, providing precise control of tape acceleration and deceleration, thus, insuring long tape life.
- Reel-to-reel tape control with independently controlled tension drives.
- Precision tape guiding, independent of cartridge characteristics and precluding contact with the oxide side of the tape.
- Snap-in load and automatic threading.
- Bidirectional read with peak transfer rate of 2000 bytes per second. High speed record search feature.
- Full interlocks to insure against operator error:
  a. File protection sensing.
  b. Cartridge in place.
  c. Cartridge in use interlock.
  d. Tape rewound, providing for rewind with or without interlock.
  e. End of tape detection.
- High density, self-clocking write and read recovery, providing maximum reliability and guarantee of drive-to-drive compatibility plus the inherent self-checking afforded by phase modulation recording.
- Full read after write check.
- In addition to the inherent advantages of a self-clocking read system, the Cogar Tape System is further complemented by the automatic compensation for apparent speed changes which can occur from physical changes to the tape itself.
- System expandability – up to eight cartridge drives can be configured with a single System 4, permitting high performance sort and file merge operations.

The Cogar System 4 contains a unique tape system, developed by Cogar, which combines the convenience and simplicity of a "snap in" self-loading cartridge with the standards of reliability and guaranteed data integrity attainable by the most advanced of the industry compatible tape drives. Utilizing the same basic design principles proven in the designs of industry compatible tape drives, the system consists of two mechanically independent tape transports, which are functionally identical and utilize an exclusive Cogar tape cartridge. The cartridge houses a reel containing 100 feet of computer grade, one mil polyester magnetic tape 150 mils wide. The cartridges are provided with a write-enable pin, to preclude erasing or writing on the tape, except when the pin is in the write-enable position. An inner reel functions independently of the outer cartridge, thus providing a true reel-to-reel tape handling mechanism. Tape threading is accomplished automatically through the use of a leader system connected to the takeup reel. The transports contain sensors to detect three tape status conditions: the presence of a cartridge properly loaded, tape not fully rewound, and end of tape. Mechanical interlocks are included to prevent cartridge removal, except when the tape is fully rewound into the reel; and to prevent tape motion, unless the cartridge is properly seated in its holder.

A write pin sensor in the C4 requires that if a tape is to be written on, the write enable pin plug must be in the proper position. Otherwise, tape will not move and no operation can be performed on that deck until a cartridge is inserted with the write pin in place.

Tape formatting, read forward/backward, and read/write checking is under processor control. Record size, interrecord gaps, check data and number of retrys are variable as functions of software. This allows the tape system to be optimized by program control, for particular user applications. The tape parameters contained in the standard Cogar software systems provide for a nominal 900 records of 136 bytes each per cartridge.

Recording density is 1600 bits per inch, phase encoded on a single track. The write track width is 80 mils, and the read width is 50 mils. The tape recovery system utilizes an energy averaging technique to determine the presence or absence of data, thus effecting an essentially infinite gain data recovery system.

Read/Write tape speed is 10 inches per second, as determined by a servo-controlled capstan which maintains a very close tape speed tolerance and allows maximum recording density. As a means of further enlarging the allowable cumulative tolerances within the tape system, the read electronics employs a servoed recovery clock, capable of tracking both intermediate and long term time displacement variations in the recovered data.

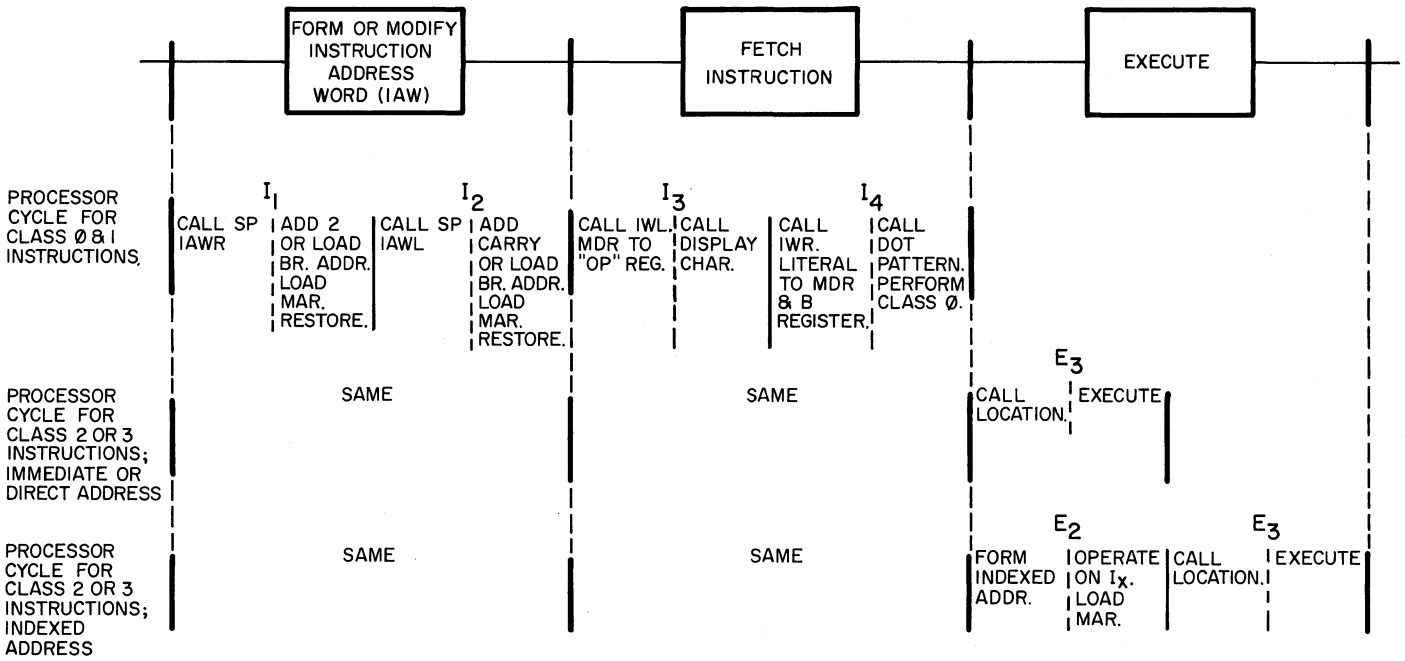
The tape transports also provide a high speed mode of 40 inches per second, that is utilized during rewind and bidirectional searches. The energy averaging detectors are used to count records for high speed searching.

The tape logic contains the hardware to allow reading backward without requiring the software to invert and shift the data. The only requirement is that a data block must be ended by a reverse read start pattern consisting of a 001 byte followed by two bytes of 000.

The tape logic also contains an 8-bit buffer that will hold a character on queue for 512 microseconds, allowing that much time for data processing before releasing the character.

Processor Architecture

The processor contained within the Cogar System 4 is fully general purpose, with a repertoire of more than 45 instructions. In addition to the conventional arithmetic and logical instructions, there is a class of powerful branch instructions that facilitate byte manipulation and sub-routine linkage. The processor design is highly memory oriented and all processor activity is memory dependent. The memory used in the Cogar System 4 is a monolithic semi-conductor memory.



PROCESSOR CYCLE PHASES

Processor Cycle

One cycle of processor operation is divided into a maximum of 6 processor subcycles (phases) that are labeled I_1, I_2, I_3, I_4, E_2, E_3. Each phase is one microsecond long.

I_1 through I_4 are the instruction phases of the processor and all four are required for every machine cycle. During I_1 and I_2 phases the address of the last instruction is retrieved from an Instruction Address Work (IAW) located in Memory. During I_3 and I_4 phases the current instruction is extracted from memory and decoded.

E_2 and E_3 are the execution phases of the processor. The E phases are conditional, based on the specific instruction being executed. Byte transfer instructions skip E_2. Branch and I/O instructions skip all E phases.

Phases I_3 and I_4 are also the display phases of the processor. One phase will locate the character to be displayed on the basis of the CRT beam position. The succeeding phase will call a segment of a dot pattern corresponding to that character and the current horizontal position of the CRT beam. The display is scanned vertically, and has access to one byte segment of dot pattern data for each character position it passes through. Seven of the eight bits of the byte contain the vertical portion of the 5x8 matrix. The specific display buffer area is presettable under program control. Any page (8 line display) or sub-page (4 line display) within the first 4 pages of Sections 0-3 of memory may be displayed.

Many of the registers used by the processor are "soft" registers and buffers located in memory. The keyboard translation table is in memory, as are the display dot matrix and the display character buffer; as well as several utility subroutines for tape and I/O control. There are seven Index Registers (IX), per 2K section of memory, of one byte each, occupying memory locations 001 through 007 of each section, that may be used for indexed addressing or as general registers. There are 16 Instruction Address Words of two bytes each, in memory that are addressed by the hardware Stack Pointer.

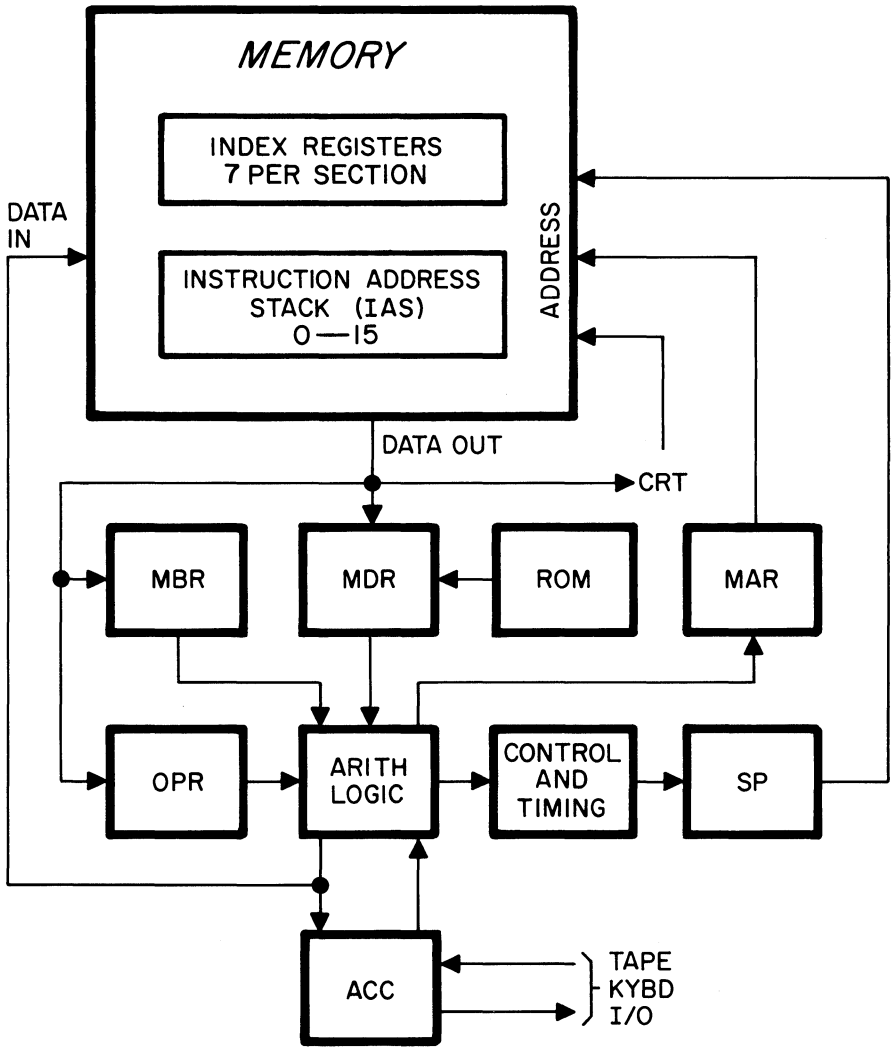
Processor Hardware

Initial program load (bootstrap) is accomplished by an 8 instruction subroutine contained in a Read Only Memory (ROM). The addressing of this Read Only Memory is congruent with main memory addresses 400_8 through 417_8 during power-on sequencing or activating the program load switch. Execution of the first stack instruction resets the bootstrap mode and returns control to main memory addressing. A switch initiated program restart causes an automatic branch to location 1000_8.

The Memory Data Register (MDR) is one byte long and is used to hold data during the formation of an effective address and during arithmetic and logical operations. The Memory Buffer Register (MBR) is one byte long and is used to hold the offset value for jump instructions, the literal value for indexing arithmetic operations and in the formation of indexed addresses. The Operation Register (OPR) receives and decodes the operand byte during phase I_3 including the address of the index register to be used (if any) or the accumulator shift count. The Memory Address Register (MAR) is 14 bits long, allowing indexed addressing of up to 16K bytes of memory.

The arithmetic and logic section of the processor executes all arithmetic, logic and compare instructions, including the overhead operations such as incrementing the index registers and the instruction address words. The accumulator is one byte long, and is the object of all arithmetic and logic operations, except those performed on index registers. The accumulator serves as the data interface for all external processor activity, except CRT refresh. The stack pointer is a 4 bit hardware counter that addresses the instruction address stack in memory.

When the processor is waiting for input (from the keyboard, for example), it enters the "stall mode." In this condition the arithmetic logic is inhibited, so that the IAW does not get incremented. In this way the processor continues to cycle, so that the display can function, no program progress is made.



SYSTEM 4 PROCESSOR

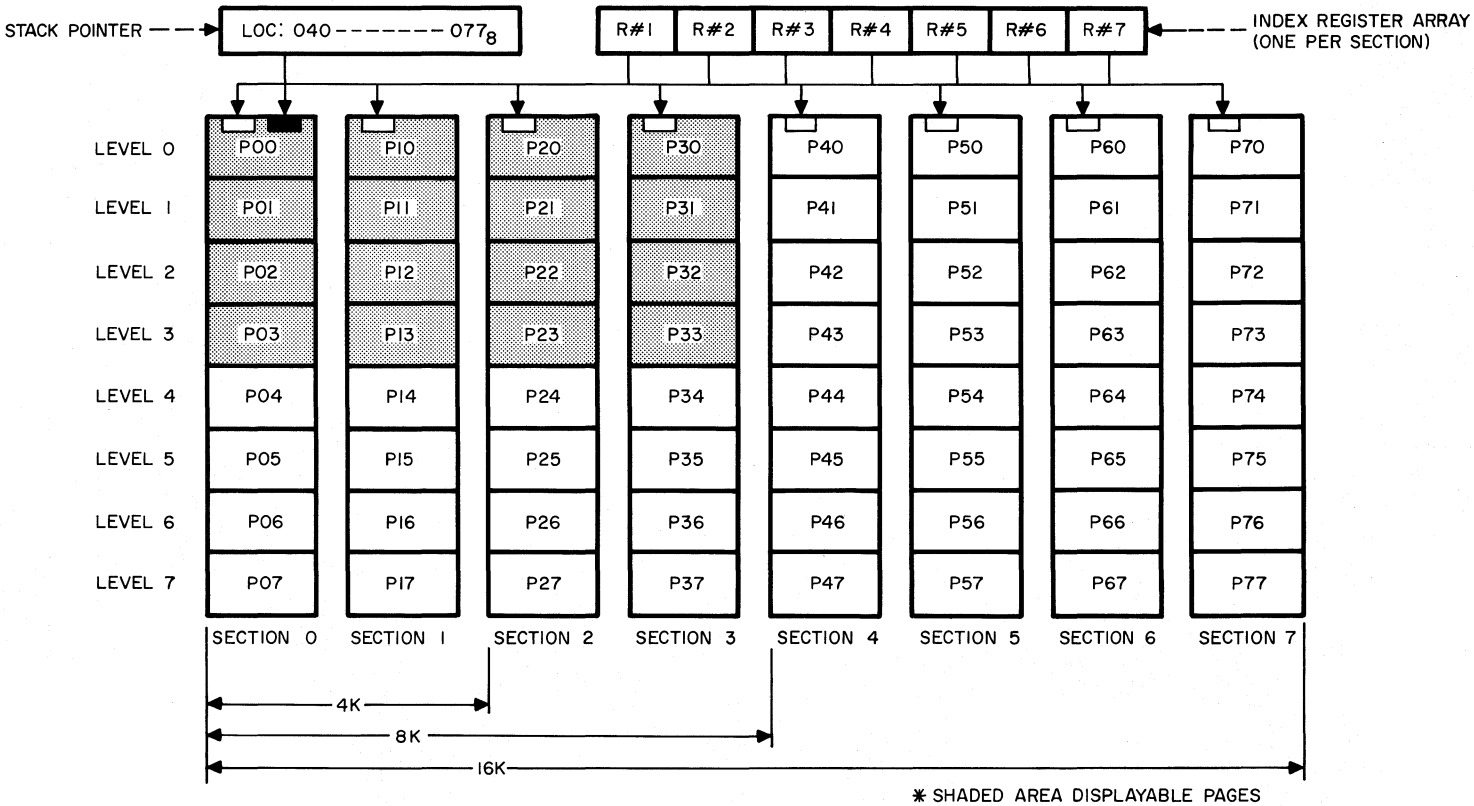
Memory

The standard Cogar System 4 is equipped with 4K bytes of monolithic memory, expandable to 8K or 16K bytes. The memory provides processor storage, display refresh, and data buffers and registers.

The memory is divided into eight Sections, each containing 2K bytes. Each Section contains eight pages, of 256 bytes each.

The Instruction Address Stack (IAS) occupies memory locations 040_8 through 077_8. Access to the stack is under control of the hardware Stack Pointer (SP) which functions modulo 10_8. The SP is incremented upon execution of a stack and branch instruction, and decremented upon execution of an exit instruction.

The current value of SP may be determined by program which facilitates the linkage of data between relocatable subroutines. By convention the linkage data would occupy contiguous locations following the last executed stack and branch instruction.



SYSTEM 4 MEMORY MAP

Instruction Set

There are four general classes of instructions utilized in the Cogar System 4. They cover all the types of actions required from a general purpose processor. Instruction formats are shown below.

Class 0: Jump Instructions
Class 1: Branch and I/O Instructions
Class 2: Transfer and Arithmetic Instructions
Class 3: Boolean and Compare Instructions

The Cogar System 4 can contain a maximum of 16K bytes of memory, requiring an instruction address word (IAW) of 14 bits. This memory capacity is divided in 8 sections of 2K bytes each. The sections are further divided into 8 pages of 256 bytes each. All Cogar System 4 operations require addressing of instructions or data, and each mode has several types of addressing that apply to it.

Instruction Addressing

Instructions may be executed sequentially, in which case one of the 16 instruction address words within the instruction address stack is incremented during phases I_1 and I_2 of each instruction cycle.

A Jump to a new instruction location uses relative addressing by ± 30 locations with respect to the current instruction.

Direct branching may be within a page or within a section, depending on the controls set by the program. In the one case only the least significant 8 bits of the IAW are changed and in the second case the least significant 11 bits are changed.

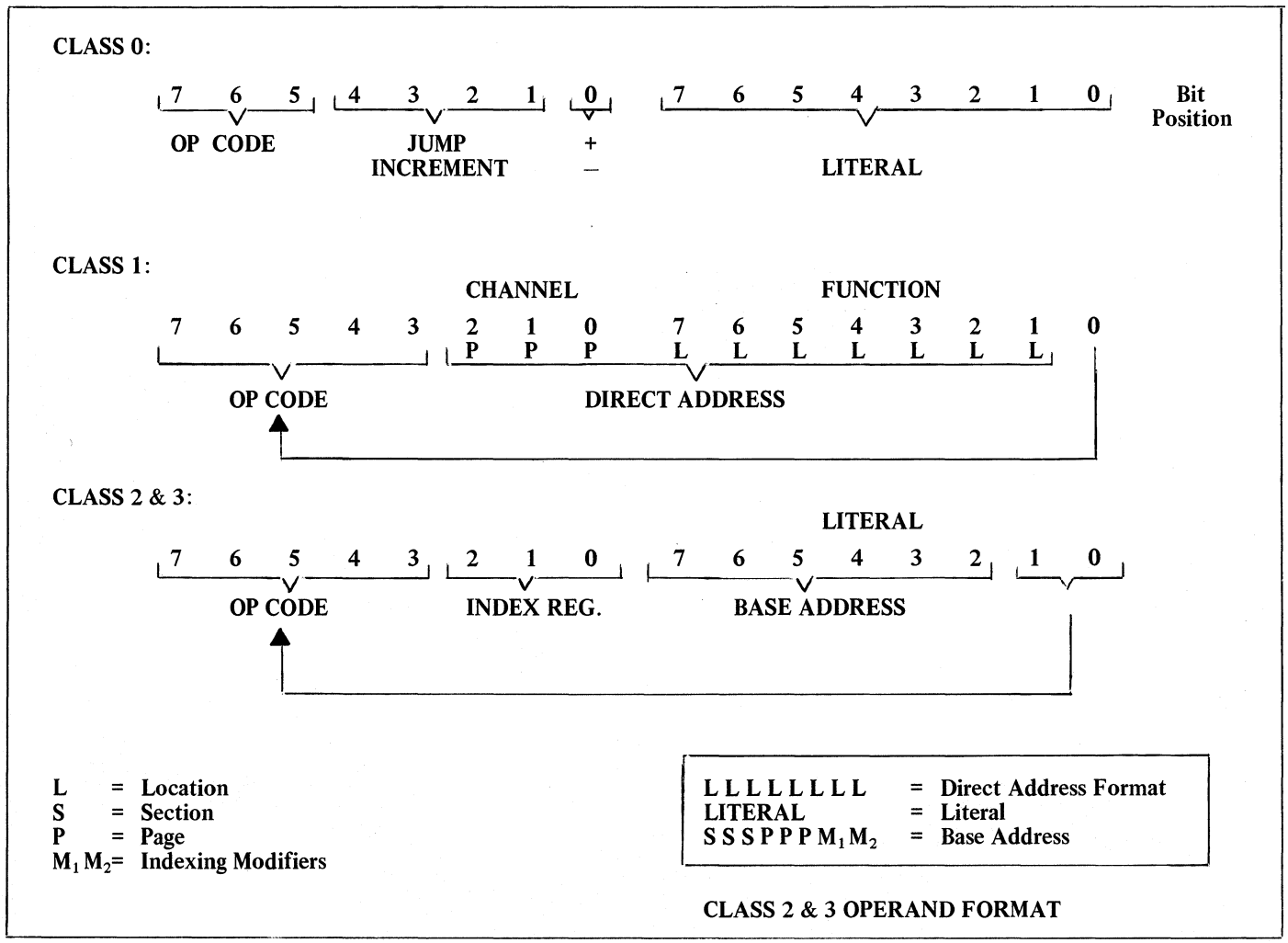
For addressing outside a Section, a set section instruction is executed. This operation changes the three bits in the IAW which designated the Section.

Data Addressing

Information may be addressed by an instruction in three modes. Immediate addressing mode assumes the instruction itself is the desired location and uses the data carried in the instruction directly.

The direct addressing mode uses the data carried in the instruction as the address of a desired memory location.

Indexed Addressing mode combines the data carried in the instruction with the contents of a specified index register to produce the address of a desired memory location. This allows addressing of a field range of 16K memory locations.



Instruction Set

	CODE	INSTRUCTION
Class 0: Jump Instructions Jump instructions transfer control within a context to a location that is relative to the current instruction location. All jump instructions are conditional and depend on the result of a test of the contents of the accumulator. The test comparison, the test mask, the jump direction and the jump increment may all be specified in the instruction.	TLJ TMJ TLX TMX	Test Literal and Jump Test Mask and Jump Test Literal and Exit Test Mask and Exit
Class 1: Branch and I/O Instructions Branch instructions transfer control outside a context to any direct address location. Direct branch instructions may be conditioned by previous compare operations. Stack and branch instructions are used to access subroutines and may be conditioned by previous compare operations. When executed, the stack and branch instruction increments the stack pointer and stores the target instruction address into the instruction address stack. The exit and the exit and branch instructions are used to return from subroutines. When executed, they decrement the stack pointer, thus changing program control to the next previous IAW. Hardware controls that are set by instructions allow branch instructions that alter only the 8 low order bits of the instruction address. This provides the capability to create page oriented subroutines that may be moved to any page of memory desired. The I/O, set section and load processor status instructions are also part of this class. They include control, status and data exchange between the processor and its interface devices. Tape channels may be selected, tape motions initiated, and read or write commanded; the keyboard may be read, or clicked; the CRT may be enabled or disabled; the I/O interface transmission may be started or stopped, and data or control bytes written. Several status checks are available for the processor to interrogate.	BRU BRE BRH BRL SBU SBE SBH SBL EXB EXU SMS SMC SSC SAC LSW LPS DPI EPI CPI	Branch Unconditional Branch on Equal Branch on High Branch on Low Stack and Branch Unconditional Stack and Branch on Equal Stack and Branch on High Stack and Branch on Low Exit and Branch Exit Unconditional Set Memory Section Set Memory Control Set Memory Section and Control Set Arithmetic Condition Load Sense Switches Load Processor Status Disable Processor Interrupt Enable Processor Interrupt Clear Processor Interrupt
Class 2: Transfer and Arithmetic Instruction This class of instructions includes the load and store operations that allow data to be moved between memory and the accumulator, or the index registers. These instructions use immediate, direct or indexed addressing modes. When loading or storing through indexed addressing, the index register used may be automatically incremented or decremented. The IWR of this instruction class may be specified as the direct address (referring to the low order page of a section), or as the base address (specifying one of 16 pages for indexed addresses), or as a literal for loading the accumulator or the index registers. The arithmetic instructions in this class include add and subtract operations on the accumulator or the index registers. Literal, direct or indexed addressing may be used. Automatic increment or decrement of index registers may be specified when using indexed address. All operations are available for use with the accumulator. Some operations may also be performed on index registers.	LDA LDX LIA STA ADA ADX SUA SUX	Load Accumulator Load Index Register Load Instruction Address Store Accumulator Add to Accumulator Add to Index Register Subtract from Accumulator Subtract from Index Register

Instruction Set

Class 3: Boolean and Compare Instructions

The Boolean instructions in this class include immediate, direct or indexed addressing of And, inclusive Or and exclusive Or operations. The literal instructions allow for up to seven right circular shifts of the accumulator prior to the execution of the literal.

The compare class of instructions compares the contents of the accumulator with a location specified by immediate, direct or indexed addressing. Any index register may be compared with a literal. The comparison results may be tested in any following instruction.

Automatic increment or decrement of an index register may be specified when using indexed addressing.

CODE	INSTRUCTION
ANA	Logical AND to Accumulator
SAN	Shift & logical AND to Accumulator
ERA	Exclusive OR to Accumulator
SER	Shift & Exclusive OR to Accumulator
IRA	Inclusive OR to Accumulator
SIR	Shift & Exclusive OR to Accumulator
CPA	Compare Accumulator
CPX	Compare Index Register

Group Instructions

This group of instructions allow complex functions to be performed by the System 4, using only a few Macro instructions. The important difference between these groups and the Class 0 through 3 instructions is that the Class instructions are directly executable by the processor, whereas the Group instructions must be interpreted and operated upon by a supervisory routine before actual execution.

However, since the Group type instruction is procedure-oriented rather than machine-oriented, each instruction causes routines composed of relatively large numbers of machine-language instructions to be executed. For example, the Group 1 instruction GET; 128, T#1, 000 calls out a routine which reads a string of characters from Tape Drive #1 and stores each character in sequential memory locations beginning at location 000. This routine is composed of approximately 75 machine instructions, and will automatically loop on itself 128 times to satisfy the single command.

	Group I
GET	Get Data (Read)
PUT	Put Data (Write)
	Group II
MOV	Move Storage to Storage
ADD	Add Storage to Storage
SUB	Subtract Storage to Storage
MUL	Multiply
DIV	Divide
	Group III
COM	Compare Storage to Storage
SEL;UNC	Select, Unconditional
SEL;LOW	Select, Low
SEL;EQL	Select, Equal
SEL;HGH	Select, High
SEL;NHG	Select, Not High
SEL;NEQ	Select, Not Equal
SEL;NLW	Select, Not Low
	Group IV
TCL	Tape Control Commands
PCL	Printer Control Commands
SET	Set Page

Programming the System 4

The language base for the Cogar System 4 is flexible, easy to learn and use, yet permits the programmer to take full advantage of the System 4's power. The Cogar Language Base is comprised of a comprehensive set of "Pre-packaged" functions to facilitate modular program construction. The Cogar Assembler provides linkage between these functions and the specialized routines necessary to a given application.

Programs are written and assembled in symbolic notation, with the final stage of the assembly effecting a merge of the specialized routines and the pre-packaged background functions. This method of assembly allows easy and rapid modification or correction of programs or the re-configuration of a program to accommodate different peripheral devices or the selection of a new or modified graphic set, or keyboard configuration.

All features of the Cogar Assembler are operable on a 4K System. Capitalizing on the high performance of the System 4 Tape Drives, an average program can be assembled in less than 12 minutes.

The packaged functions are available to the programmer from a Library Tape which provides for automatic retrieval and filing of specific functions. The library contains a standard set of subroutines for:

- Controlling the various peripherals
- Keyboard supervision
- Display graphics
- String oriented macros including signed arithmetic
- Communications

The programmer has complete freedom in the inter-mixing of machine language statements and macro-functions, with linkages provided by the assembler.

The sample subroutine shown above illustrates the ease with which a relatively complex function may be programmed,

```
PPP-LLL:  MP1-MP2-MP3-MP4. E  SEQ.NO. LAB: VERB   OPERANDS        COMMENTS

                               01-010. RDD: EQU: P00, 009.       READ DECK NUMBER
                               01-020. RDF: EQU: P06, 000.       CARTRIDGE READ SUBROUTINE
                               01-030. BSF: EQU: P06, 030.       READ BACKSPACE SUBROUTINE
                               01-040. BSP: EQU: P06, 196.       TIMED BACKSPACE SUBROUTINE
                               01-050.      ORG: P01, 000.
                              *01-060.
                              *01-070. READ ROUTINE ENTRY POINT
P01-000:  230-011.             01-080. RDT: STA, R#0; RDD.       SAVE READ DECK
P01-002:  126-000.             01-090.      SBU; RDF.            READ TAPE RECORD
P01-004:  111-010.             01-100.      BRH; ERR.            READ ERROR?...YES
P01-006:  140-000.             01-110.      EXU; 000.            NO - RETURN
                              *01-120.
                              *01-130. ERROR RECOVERY HANDLER
P01-010:  210-004.             01-140. ERR: LDA, R#0; R#4.       LOAD READ STATUS
P01-012:  052-010.             01-150.      TMJ, +10; OCT:010.   TAPE RUNAWAY?
P01-014:  173-013.             01-160.      IOC, C#3; 013.       NO - SOUND ALARM
P01-016:  173-207.             01-170.      IOC, C#3; 207.       RESPONSE FROM KEYBOARD?
P01-020:  101-030.             01-180.      BRU; CHK.            YES - CHECK IT
P01-022:  101-014.             01-190.      BRU; *-6.            NO - WAIT FOR KEY
                              *01-200.
                              *02-010. TAPE RUNAWAY ROUTINE
P01-024:  173-013.             02-020.      IOC, C#3; 013.       SOUND THE ALARM
P01-026:  101-024.             02-030.      BRU; *-2.            NO RECOVERY FOR TAPE RUNAWAY
                              *02-040.
                              *02-050. CHECK KEYBOARD RESPONSE
P01-030:  006-032.             02-060. CHK: TLJ, +06; OCT:032.   ERROR KEY?...YES
P01-032:  024-232.             02-070.      TLJ, +20; OCT:232.   CTRL + ERROR KEY? YES
P01-034:  101-014.             02-080.      BRU; ERR+4.          NEITHER - GET A VALID RESPONSE
                              *02-090.
                              *02-100. ERROR KEY DEPRESSED: RETRY THE READ
P01-036:  210-004.             02-110.      LDA, R#0; R#4.       LOAD READ STATUS
P01-040:  044-001.             02-120.      TMJ, +04; OCT:001.   WAS IT A READ ERROR?
P01-042:  101-046.             02-130.      BRU; *+4.            NO - HANDLE RECORD
                              *02-140.
                              *02-150. RETRY READ FOR READ ERROR ON RECORD.
                              *02-160.   BACKSPACE TWO RECORDS AND REREAD.
P01-044:  126-304.             02-170.      SBU: BSP.            TIMED BACKSPACE
                              *02-180.
                              *02-190. RETRY READ FOR RECORD SEQUENCE ERROR.
                              *02-200.   BACKSPACE ONE RECORD AND REREAD.
P01-046:  210-011.             03-010.      LDA, R#0; RDD.       LOAD DRIVE NUMBER
P01-050:  126-036.             03-020.      SBU; BSF.            READ BACKSPACE
P01-052:  210-011.             03-030.      LDA, R#0; RDD.       LOAD DRIVE NUMBER
P01-054:  101-002.             03-040.      BRU: RDT+2.          TRY READ AGAIN
                              *03-050.
                              *03-060. CTRL + ERROR KEY DEPRESSED: BYPASS ERROR
P01-056:  126-304.             03-070.      SBU; BSP.            TIMED BACKSPACE
P01-060:  210-011.             03-080.      LDA, R#0; RDD.       LOAD DRIVE NUMBER
P01-062:  360-200.             03-090.      IRA, R#0; OCT:200.   SET FOR NO SEQUENCE CHECK
P01-064:  101-002.             03-100.      BRU; RDT+2.          READ AND BYPASS
```

using the Cogar Language Base. This handler subroutine will read a record from tape, and provides all the necessary error recovery and operator interface functions. The actual Read routine is contained in another part of the main program. If an error occurs, this subroutine detects the type of error (read error, sequence error, or tape runaway), sounds the alarm to alert the operator, and waits for a valid operator response from the keyboard. If no error occurs, this subroutine returns control to the main program after the record is read.

If an error has occurred, the subroutine checks the operator's key input in response to the error, and proceeds accordingly. As long as the error is not a tape runaway, the subroutine gives the operator the prerogative to call for a read-retry (depression of the ERROR key), or to skip the record and go on to read the next sequential record on the tape (depression of the CTRL and ERROR keys).

Application Packages

Data Entry

The Cogar Data Entry program is contained on a self-loading tape, and provides the user with the ability to record, verify, and modify information. The program is designed to provide complete operator/machine interface at all times, including the notification of the operator in case of an entry error. All necessary error-recovery capabilities are included. Entry of formatted or unformatted data is permitted, at 120 characters per tape block. After verification, the data may be transferred to a standard ½ inch, 9 track compatible tape, using this program.

General Ledger Print

This program provides hard copy output of accounting data which has been entered on tape. The output formats include: General Ledger Reports, a detailed list of transaction totals within each account, and a summary report of the total of each account. Year-to-date totals are included on each report. As a report is being printed, a new year-to-date tape is created, containing a summary record with the new month's total and year-to-date amount for each account. The program may also be used to tabulate the General Ledger tapes and display the year-to-date final totals, without printing.

Teletype Simulator

This program allows the Cogar System 4 to provide a total simulation of the ASR Teletype capability. Low speed (10 – 60 cps) asynchronous terminal communications with print, tape input, and tape output capabilities are included. The operator retains complete control of all peripheral devices in either the Local or the On-Line mode. The status of the simulator is displayed at all times.

Communications

The Communications program allows the transfer of data records between two Cogar System 4 processors. Data is carried over standard switched telephone lines, through a modem or acoustic coupler. Operator instructions are displayed, and provisions for complete error detection, operator alert and error recovery are included. The user may select transmission rates of 1200 or 1800 baud.

Binary Synchronous Communications

This program allows communication with a remote IBM 360/370 system, in a binary synchronous mode, over switched networks. This added-on capability allows System 4 users to transmit accumulated data to a remote computer for collection purposes, or on-line updating. As a receiving station, the System 4 will receive records from the IBM 360/370 station, and write them to tape in EBCDIC code. The data may then be processed by the System 4 or printed out in the off-line mode.

Programmer's Utilities

Cogar Corporation has developed a comprehensive set of pre-packaged functions, to allow the user to generate and execute his own programs on the System 4 processor. Step-by-step supervisory messages are displayed during the utilization of each of these functions, to guide the operator in their use.
some of these functions
description of their uses is

Batch Assembler

This function allows the programmer to write his program in symbolic notation, (along with comments for each instruction) and preserve the program on tape in symbolic. The symbolic notation is then automatically transposed into machine language by the Batch Assembler.

The assembler also provides diagnostics to inform the user of coding errors in the program, as well as handling the controls, translations and linkages to other operational functions necessary to the proper execution of the program.

Standard Dot Matrix

The commonly used characters corresponding to a normal key punch keyboard are provided in a loadable dot matrix, for the user's convenience. The visual display uses a 5 x 8 dot matrix to form each display character, and has a cursor control with each character. However, the user has the option to change the dot matrix to suit his particular requirements, to allow any shape for the 5 x 8 character matrix. A self-loading "Dot Pattern Conversion" program is available to the user to perform this operation if desired.

Standard Translate Table

The Cogar System 4 is designed to provide code hardware transparency. The codes generated by the keyboard, for example, correspond not to the key character, but to the key location on the keyboard. A Translate Table is provided, to convert the key code into a character code. The user may modify the Translate Table, to produce any desired code for any key. Thus, any key may be translated into any desired code and any dot matrix pattern may be displayed for a given character code. These functions are directly under software control and are therefore available to the programmer.

Basic Backgrounds

The Basic Backgrounds contain the routines necessary to load the user's assembled program into the machine and execute it. Two types of Basic Backgrounds are available to the user, which may be selectively retrieved from a Cogar Library tape. Selection of the background used is dependent on whether the user's program contains only instructions which are directly executable by the machine, or whether some instructions in the program require the machine to operate on them interpretively. Information concerning the selection and content of the Basic Backgrounds is contained in the "Standard Cogar Library Functions" manual.

Filing and Copying

The programmer is provided with functions which permit the filing of his routines onto tape in an orderly manner, to create his own specialized Library. These routines may then be retrieved when desired, and utilized in other programs, without having to be re-assembled Up to ten selected routines may be retrieved in one pass and inserted into another program in user designated locations.

The Library may be updated, altered, or reorganized quickly and easily; or may be copied to another tape in its entirety or in selected portions. Also, the Table of Contents of the Library may be displayed and reviewed at any time. The programmer thus has the ability to catalog any number of quickly-recallable routines (as complete files) which are pre-assembled and immediately executable in newly generated programs.

Data Sort/Merge

The Sort/Merge program provides the user the ability to perform a three or four tape sort or merge of data records contained on the Cogar mini-tapes or on the 9-track compatible tape drive. Three fields of any length may be sorted or merged, in ascending sequence.

Functional Routines

A library of functional routines is available, which may be selectively retrieved by the programmer for use in the execution of his program. The selected routines, once retrieved from the Library Tape, are inserted into the Basic Background. A specialized Operational Background is thus created by the programmer, to allow his program to be effectively executed without being penalized by having memory space occupied by unrequired routines. Information concerning the selections and function of each routine is contained in the "Standard Cogar Library Functions" manual. A partial listing of the function of these routines is as follows:

1. Read and Write on Mini-Tape.
2. Allow read from Mini-Tape into various areas of memory.
3. Allow write from Mini-Tape into various areas of memory.
4. Translate the C4 code into EBCDIC and provide hard copy at 197 characters per second from the Line Printer.
5. Translate the C4 Code into USAC11 code and provide hard copy at 165 characters per second from the Centronics Printer.
6. Translate the C4 Code into IBM Selectric compatible code and provide hard copy from the IBM 735 Selectric typewriter
7. Read or Write on a 9-track compatible tape drive.
8. Allow printing of a single character on a Selectric typewriter when operating in a time-share mode.
9. Multiply/Divide function and controls.
10. Input/Output supervisor for interpretive type commands.
11. Execute N times any instruction entered from the keyboard with program resident in the machine.

Program Trace

This utility provides the programmer with a powerful tool when debugging his program. The user may select any start point for execution of his program, and a temporary stop at any point. After stopping, the contents of the next sequential memory address is displayed, along with the contents of the accumulator, index registers, stack pointer, and the condition register. The user may then execute sequential single instructions, or "patch" the program where desired.

High Speed Record Search

This function allows the user to locate and display any record on tape, in a high speed (40 ips) mode. After a selected record has been located and displayed, its location is used as a starting point to search for the next record to be located. This feature eliminates the need for tape rewind after each search, and considerably reduces the time required to search for multiple records.

Peripherals

A comprehensive set of peripheral devices is available with the Cogar System 4. These peripherals have been chosen to allow the greatest flexibility in their configuration in a system utilizing the System 4, to satisfy the most demanding application requirements.

Printer Adapters

Interfaces are available for a variety of printers using either the parallel or the serial I/O channel, as dictated by system requirements. Each of these adapters is packaged in a peripheral enclosure, which contains its own power supply and input-output cables. Use of the parallel I/O for printer attachment permits concurrent operation of the printer and compatible tape units which are connected via the serial I/O channel, as well as permitting higher printing rates. Interfaces for the Centronics Printer and for the IBM 735 Printer are available on request. Interfaces for other printers are currently being developed. Inquiries regarding special application interfaces should be directed to Cogar Corporation. The interfaces presently available are designed to accommodate the following types of printers:

Centronics Printer Characteristics
Print Speed: 165 Char/second
Line Width: 132 Characters
IBM 735 Printer Characteristics
Print Speed: 15 Char/second
Line Width: 132 Characters

Mini-Tape Dual Drives

These self-contained units are designed to efficiently increase the tape handling capabilities of the System 4. Each unit contains two tape drives, drive motor power supply, and speed control electronics. The increased tape handling capability resulting from the use of the Dual Drives with the Cogar System 4 allows the performance of tasks such as record Sort and Merge, general purpose accounting procedures, updating of multiple files, etc. One, two or three Dual Drives may be connected in series with the System 4, expanding the total tape handling capability of the system to eight tape drives. Instructions for accessing and controlling the Dual Drives through the System 4 are contained in the Cogar software for the System 4.

Compatible Maxi-Tape Units

Information interchange between the System 4 and other data processing systems may be accomplished using a variety of compatible Maxi-Tape units including:

- 556 bits/inch, 7 track
- 800 bits/inch, 9 track (7½" reel)
- 800 bits/inch, 9 track (10" reel)
- 1600 bits/inch, 9 track

In addition, the Cogar software permits the use of these units for the sorting and merging of files, and for storage of large data banks. Connectable via the serial I/O channel of the System 4, each unit contains its own serial I/O interface, and may be address-selectable.

Cogar Dual Drives

Communications Adapter Enclosure

The parallel I/O channel can accommodate up to four separate communications adapters; namely, the Batch Communications Adapter, the Bisynchronous Communications Adapter, the Teletype Simulator Adapter, and the C24 Control Unit (or the IBM 735 Adapter). Any or all of these adapters may be packaged in a separate enclosure, which contains its own power supply and interface connections to the System 4 and to the various modems. A single cable connects all of the adaptors in the enclosure to the parallel I/O channel in the System 4.

Communications Adapter Enclosure

C24 Control Unit

The Cogar System C24 Control Unit accomplishes the necessary interchange of control signals between a Cogar System 4 and a System 360/370, to permit reliable information exchange between Cogar and IBM systems. The combination of the System 4 and the C24 Control Unit provides maximum system transparency by allowing the System 4 to simulate the characteristics of the desired IBM peripheral device.

Up to sixteen device addresses can be recognized by the Control Unit, through the "multiplexor" or "selector" channel of the IBM systems. The C24 Control Unit conforms to all the electrical, mechanical, and cabling considerations and specifications of interfacing as defined in the OEMI manual "IBM System/360 and System/370 I/O Interface Channel to Control Unit Original Equipment Manufacturer's Information."

Utilizing the 2803 simulation package, the System 4 will respond to all tape control commands with the exception of "Read Backward." Operations are functionally equivalent to an on-line 2400 Series Tape Drive. Necessary operator instructions and status information are provided via the System 4 CRT display.

Cogar System C24

Numeric Keypad

A numeric keypad containing the 0 through 9 digits, as well as a key and a minus key which are set on the pad in the same configuration as an adding machine key layout may be plugged in to a connector provided on the System 4. This feature expedites the entering of numeric data by operators who are accustomed to accounting machine-type keyboards, and obviates the requirement of retraining to familiarize the operator with the keypunch keyboard.

Test Console

A portable, light-weight, free standing unit which contains all display indicators and control switches on a panel which measures 11 inches high and 11 inches wide. The Test Console allows the Cogar System 4 to be completely controlled externally, and permits observation of pertinent register contents at selected times within the processing cycle of an instruction.

Specification Summary

Size	10 inches high (25 cm) 18.5 inches wide (47 cm) 24 inches deep (60 cm)
Weight	52 pounds (23.6 kg)
Power	115 VAC ±10%, 220 VAC ±10% 48 to 62 Hz 2.5 amps average
Environment	10% to 80% relative humidity without condensation 60°F to 95°F Operating Temperature 0°F to 150°F Storage Temperature
Ventilation	30 cubic feet per minute air flow 4 inches air flow clearance on all sides 1000 BTU per hour heat dissipation
Processor	45 instruction types plus I/O 3 to 6 μs instruction cycle time 1 Accumulator 7 Index Registers per 2K of memory 16 Member Instruction Address Stack 1 Stack Pointer Hardware Bootstrap Loader
Memory	16K bytes capacity Random Access Read/Write Non-Destructive Read-Out Monolithic Semiconductor
Keyboard	Software configurable Hall effect keys N-Key rollover capability Audible cue
Visual Display	5 inch CRT 4 or 8 line display, with interleave capability 32 characters per line 5 x 8 matrix under program control
Tape System	10 ips write tape speed 1600 bpi density, phase modulation 2 mechanically independent transports Read after Write, CRC, phase checks Automatic threading Write interlock switch Rewind: 40 ips rewind and forward or rewind search
Tape Cartridges	100 ft. computer grade tape 900 records of 136 characters each Write/Erase Protection

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